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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/26/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/351,544	CARNS ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the etching the bottom electrode layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what the statement "wherein to forming said insulating layer by deposition, an anneal is performed" means in the context of forming the insulating layer. Is an anneal performed before, after or during the deposition of the insulating layer?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 3, 8, 12 – 16, 19 – 21, 25, 36, 39 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Kayanuma et al. (USPAT 5397729, Kayanuma).

With regard to claim 1, Kayanuma discloses in figures 4a – 4f and column 10, lines 38 – 40 forming a capacitor in an integrated circuit. Kayanuma discloses in figure 4a forming a bottom electrode layer (52) on a semiconductor body (50). Kayanuma discloses in figure 4a forming a dielectric layer (53) over at least a portion of the bottom electrode. Kayanuma discloses in figure 4a forming a top electrode layer (54) over at least a portion of the dielectric layer. Kayanuma discloses in figure 4b and column 10, lines 38 – 40 removing a portion of the top electrode layer to expose a portion of the dielectric layer and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode. Kayanuma discloses in figure 4c and column 10, lines 38 – 40 subsequently forming a conformal insulating layer (57) over at least a portion of the exposed portion of the bottom electrode layer proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer. Kayanuma discloses in figure 4c – 4f subsequently etching the bottom electrode layer.

With regard to claim 2, Kayanuma discloses in figure 4e further comprising forming a non-insulating layer (59) over at least a portion of the resultant structure subsequent to forming the conformal insulating layer and prior to etching the bottom electrode layer.

With regard to claim 3, Kayanuma discloses in figures 4a – 4f and column 10, lines 38 – 40 forming a capacitor in an integrated circuit. Kayanuma discloses in figure 4a forming a bottom electrode layer (52) on a semiconductor body (50). Kayanuma discloses in figure 4a forming a dielectric layer (53) over at least a portion of the bottom electrode. Kayanuma discloses in figure 4a forming a top electrode layer (54) over at least a portion of the dielectric layer. Kayanuma discloses in figure 4b and column 10, lines 38 – 40 removing a portion of the

top electrode layer to expose a portion of the dielectric layer and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode. Kayanuma discloses in figure 4c and column 10, lines 38 – 40 subsequently forming a conformal insulating layer (57) over at least a portion of the exposed portion of the bottom electrode layer proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer. Kayanuma discloses in figure 4c – 4f subsequently etching the bottom electrode layer. Kayanuma discloses in figure 4e forming an anti-reflective layer (ARL) (59) over at least a portion of the resultant structure subsequent to forming the conformal insulating layer.

With regard to claim 8, Kayanuma discloses in figure 4e wherein the ARL is an anti-reflective coating.

With regard to claim 12, Kayanuma discloses in figure 4f wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

In regard to claim 13, Kayanuma discloses in figures 4a – 4f and column 10, lines 38 – 40 forming a capacitor in an integrated circuit. Kayanuma discloses in figure 4a forming a bottom electrode layer (52) on a semiconductor body (50). Kayanuma discloses in figure 4a forming a dielectric layer (53) over at least a portion of the bottom electrode. Kayanuma discloses in figure 4a forming a top electrode layer (54) over at least a portion of the dielectric layer. Kayanuma discloses in figure 4b and column 10, lines 38 – 40 removing a portion of the top electrode layer to expose a portion of the dielectric layer. Kayanuma discloses in figure 4c and column 10, lines 38 – 40 forming an insulating layer (57) over at least a portion of the top electrode layer and the

exposed portion of the dielectric layer. Kayanuma discloses in figure 4d removing a portion of the insulating layer and a portion of the dielectric layer, thereby exposing at least a portion of the lower electrode and forming side wall spacers , wherein the side wall spacers are formed on the side walls of the top electrode and of the inter electrode region of the dielectric.

With regard to claim 14, Kayanuma discloses in figure 4e forming a non-insulating layer (59) over at least a portion of the resultant structure subsequent removing a portion of the insulating layer and a portion of the dielectric layer.

With regard to claim 15, Kayanuma discloses in figure 4e wherein the non-insulating layer is an anti-reflective layer (ARL).

With regard to claim 16, Kayanuma discloses in column 8, lines 48 – 52 wherein the insulating layer is formed by deposition.

With regard to claim 19, Kayanuma discloses in column 8, lines 48 – 52 wherein the insulating layer is an oxide layer with a thickness of 1000 Å.

With regard to claim 20, Kayanuma discloses in column 8, lines 33 – 36 and 48 – 52 wherein the side wall spacers have a width in the range of about 1450 Å.

With regard to claim 21, Kayanuma discloses in figure 4e wherein the ARL is an anti-reflective coating.

With regard to claim 25, Kayanuma discloses in figure 4f wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 36, Kayanuma discloses in figure 4a forming a conductive layer on a semiconductor body. Kayanuma discloses in figure 4b forming a capacitor structure

comprising: a top electrode over a portion of the conductive layer; and a dielectric layer between the top electrode and the conductive layer. Kayanuma discloses in figure 4c and column 10, lines 38 – 40 forming a conformal insulating layer over the capacitor structure and at least a portion of the conductive layer proximate to the capacitor structure. Kayanuma discloses in figure 4d forming an anti-reflective layer (ARL) over at least a portion of the structure resultant from the forming a conformal layer. Kayanuma discloses in figure 4d forming a patterned mask over the structure resultant from the forming an ARL. Kayanuma discloses in figure 4f etching the conductive layer using the patterned mask.

With regard to claim 39, Kayanuma discloses in figure 4f wherein the conductive layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 40, Kayanuma discloses in figure 4a forming a conductive layer on a semiconductor body. Kayanuma discloses in figures 4a – 4f providing a process flow for etching the conductive layer, whereby the gates of one of more transistors are formed, the flow including a photolithographic process. Kayanuma discloses in figure 4e forming an anti-reflective layer (ARL) over at least a portion of the conductive layer. Kayanuma discloses in figure 4e forming a patterned mask over the ARL, wherein the photolithographic process is optimized for forming the gates. Kayanuma discloses in figure 4a – 4d performing a capacitor formation process. Kayanuma discloses in figures 4a and 4b forming one or more capacitor structures, each comprising a top electrode over a portion of the conductive layer and a dielectric layer between the top electrode and the conductive layer. Kayanuma discloses in figures 4c – 4e forming a conformal insulating layer over the capacitor structures and at least a portion of the conductive layer proximate to capacitor structures, therein the capacitor formation process is

performed prior to forming the ARL, whereby the ARL is additionally formed over the capacitor structures, and whereby the conformal insulating layer is formed such that the provided process flow is unaltered. Kayanuma discloses in figure 4f etching the conductive layer according to the process flow, whereby the lower electrodes of the capacitor structures and the gates are formed.

5. Claims 26, 27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al. (USPAT 5618749, Takahashi).

With regard to claim 26, Takahashi discloses in figures 6 – 10 a method of forming a capacitor in an integrated circuit. Takahashi discloses in figure 6 forming a bottom electrode layer (2) on a semiconductor body (100). Takahashi discloses in figure 7 forming a dielectric layer (1) over at least a portion of the bottom electrode. Takahashi discloses in figure 7 forming a top electrode layer (6a) over at least a portion of the dielectric layer. Takahashi discloses in figure 8 removing a portion of the top electrode layer to expose a portion of the dielectric layer. Takahashi discloses in figure 9 forming an anti-reflective layer (ARL) (6b) over at least a portion of the top electrode and the exposed portion of the dielectric layer. Takahashi discloses in figure 10 subsequently removing a portion of the exposed portion of the dielectric layer and a portion of the bottom electrode layer, thereby exposing at least a portion of the semiconductor body and forming one or more capacitors.

With regard to claim 27, Takahashi discloses in figure 10 wherein the ARL is an anti-reflective coating.

With regard to claim 30, Takahashi discloses in figure 10 wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 – 7 and 31 – 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma in view of Wang et al. (USPAT 5545585, Wang).

With regard to claim 4, Kayanuma discloses in figures 4a – 4f and column 10, lines 38 – 40 forming a capacitor in an integrated circuit. Kayanuma discloses in figure 4a forming a bottom electrode layer (52) on a semiconductor body (50). Kayanuma discloses in figure 4a forming a dielectric layer (53) over at least a portion of the bottom electrode. Kayanuma discloses in figure 4a forming a top electrode layer (54) over at least a portion of the dielectric layer. Kayanuma discloses in figure 4b and column 10, lines 38 – 40 removing a portion of the top electrode layer to expose a portion of the dielectric layer and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode. Kayanuma discloses in figure 4c and column 10, lines 38 – 40 subsequently forming a conformal insulating layer (57) over at least a portion of the exposed portion of the bottom electrode layer

proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer. Kayanuma discloses in figure 4c – 4f forming an anti-reflective layer (ARL) (59) over at least a portion of the resultant structure subsequent to forming the conformal insulating layer. Kayanuma does not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Kayanuma in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 5, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 6, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the thermal process is a thermal oxidation. Kayanuma and Wang do not disclose that the conformal insulating layer is formed in a rapid thermal process that is a rapid thermal oxidation performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It is well known in the art to use a rapid thermal process in the production of a thermal oxide layer that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use a rapid thermal process that has parameters of from 10 to 60 seconds and at a temperature in the range from

850°C the 1050°C to form the conformal insulating layer of Kayanuma and Wang in order to choose a method that is widely used and understood in the art and produces a consistent and reliable oxide layer.

With regard to claim 7, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is formed by deposition.

With regard to claim 31, Kayanuma discloses in figure 4a forming a conductive layer on a semiconductor body. Kayanuma discloses in figure 4b forming a capacitor structure comprising: a top electrode over a portion of the conductive layer; and a dielectric layer between the top electrode and the conductive layer. Kayanuma discloses in figure 4c and column 10, lines 38 – 40 forming a conformal insulating layer over the capacitor structure and at least a portion of the conductive layer proximate to the capacitor structure. Kayanuma does not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Kayanuma in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 32, Kayanuma discloses in figure 4e forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming the conformal insulating layer.

With regard to claim 33, Kayanuma discloses in figure 4e wherein the non-insulating layer is an anti-reflective layer (ARL).

With regard to claim 34, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 35, Kayanuma discloses in figure 4f wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

7. Claims 17, 18, 37, 38, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma as applied to claims 15, 16, 36 and 40 above, and further in view of Wang.

With regard to claim 17, as far as the examiner can ascertain the combination of Kayanuma and Wang would read on the claimed invention in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 18, Kayanuma does not disclose wherein the insulating layer is grown. Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 growing an insulating layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use method of growing an insulating layer of Wang in the method of Kayanuma in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 37 and 41, Kayanuma does not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Kayanuma in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 38 and 42, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

8. Claims 9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma as applied to claims 3 and 15 above, and further in view of Noda et al. (USPAT 5068697, Noda).

With regard to claims 9 and 22, Kayanuma discloses in column 9, lines 11 – 15 using a metal silicide film as the ARL. Kayanuma does not disclose using an ARL that is titanium nitride. Noda discloses in column 4, lines 32 – 35 an ARL that is titanium nitride. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the ARL that is titanium nitride of Noda in the method of Kayanuma in order to form the ARL of a material having low reflectance as stated by Noda in column 8, lines 14 – 17.

9. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi as applied to claim 26 above, and further in view of Noda.

With regard to claims 9, 22, Takahashi discloses in column 7, lines 58 – 62 using a metal silicide film as the ARL. Takahashi does not disclose using an ARL that is titanium nitride. Noda discloses in column 4, lines 32 – 35 an ARL that is titanium nitride. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the ARL that is titanium nitride of Noda in the method of Takahashi in order to form the ARL of a material having low reflectance as stated by Noda in column 8, lines 14 – 17.

10. Claims 10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma as applied to claims 3 and 15 above, and further in view of Doan et al. (USPAT 6208033, Doan).

With regard to claims 10 and 23, Kayanuma discloses in column 6, lines 59 – 64 that the ARL is a titanium silicide layer. Kayanuma does not disclose depositing the ARL by plasma enhance chemical vapor deposition (PECVD). Doan discloses in column 4, lines 13 – 16 depositing an ARL of titanium silicide by PECVD. It would have been obvious to use the PECVD of Doan in the method of Kayanuma in order to create a layer with decreased contact resistance as stated by Doan in column 1, lines 16 – 22 and column 2, lines 15 – 24. The antireflective coating of Kayanuma and Doan could be called a plasma enhance chemical vapor deposition anti-reflective layer (PEARL).

11. Claims 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi as applied to claims 26 above, and further in view of Doan et al. (USPAT 6208033, Doan).

With regard to claims 10 and 23, Takahashi discloses in column 8, lines 8 – 9 that the ARL is a titanium silicide layer. Takahashi does not disclose depositing the ARL by plasma enhance chemical vapor deposition (PECVD). Doan discloses in column 4, lines 13 – 16 depositing an ARL of titanium silicide by PECVD. It would have been obvious to use the PECVD of Doan in the method of Takahashi in order to create a layer with decreased contact resistance as stated by Doan in column 1, lines 16 – 22 and column 2, lines 15 – 24. The antireflective coating of Takahashi and Doan could be called a plasma enhance chemical vapor deposition anti-reflective layer (PEARL).

12. Claims 11 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma and Doan as applied to claims 10 and 23 above, and further in view of Tsai et al. (USPAT 5728619, Tsai).

Kayanuma and Tsai do not disclose a thickness of the titanium silicide layer that is in the range from 300 to 400 angstroms. Tsai discloses in column 8, lines 61 – 67 a titanium silicide thickness of about 400 angstroms. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the titanium silicide thickness of Tsai in the method of Kayanuma and Doan in order to form a layer of titanium silicide with good electrical properties that is sufficient at the dimensions of the integrated circuit design choice.

13. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi and Doan as applied to claims 29 above, and further in view of Tsai et al. (USPAT 5728619, Tsai).

Takahashi and Tsai do not disclose a thickness of the titanium silicide layer that is in the range from 300 to 400 angstroms. Tsai discloses in column 8, lines 61 – 67 a titanium silicide thickness of about 400 angstroms. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the titanium silicide thickness of Tsai in the method of Takahashi and Doan in order to form a layer of titanium silicide with good electrical properties that is sufficient at the dimensions of the integrated circuit design choice.

Response to Arguments

14. Applicant's arguments with respect to claims 1 – 42 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
November 7, 2001

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